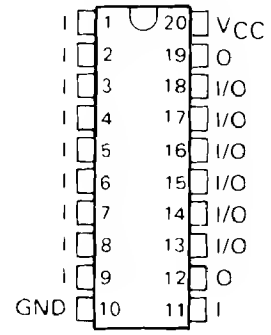
TIBPAL16L8-5C, TIBPAL16R4-5C, TIBPAL16R6-5C, TIBPAL16R8-5C
TIBPAL16L8-7M, TIBPAL16R4-7M, TIBPAL16R6-7M, TIBPAL16R8-7M
HIGH-PERFORMANCE *IMPACT-X*™ *PAL*® CIRCUITS

D3359, OCTOBER 1989—REVISED MAY 1990

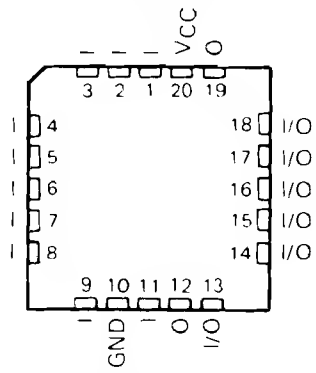
- High-Performance Operation:
  - f_{max} (no feedback)
    - TIBPAL16R'-5C Series . . . 125 MHz
    - TIBPAL16R'-7M Series . . . 100 MHz
  - f_{max} (internal feedback)
    - TIBPAL16R'-5C Series . . . 125 MHz
    - TIBPAL16R'-7M Series . . . 100 MHz
  - f_{max} (external feedback)
    - TIBPAL16R'-5C Series . . . 115 MHz
    - TIBPAL16R'-7M Series . . . 74 MHz
  - Propagation Delay
    - TIBPAL16L'-5C . . . 5 ns Max
    - TIBPAL16L'-7M . . . 7 ns Max
- Functionally Equivalent, but Faster than Existing 20-Pin PALs
- Preload Capability on Output Registers Simplifies Testing
- Power-Up Clear on Registered Devices (All Register Outputs are Set Low, but Voltage Levels at the Output Pins Go High)
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Security Fuse Prevents Duplication

DEVICE	INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL16L8	10	2	0	6
PAL16R4	8	0	4 (3-state)	4
PAL16R6	8	0	6 (3-state)	2
PAL16R8	8	0	8 (3-state)	0

TIBPAL16L8'
C SUFFIX . . . J OR N PACKAGE
M SUFFIX . . . J PACKAGE
(TOP VIEW)



TIBPAL16L8'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE
(TOP VIEW)



Pin assignments in operating mode

description

These Programmable Array Logic devices feature the highest speed yet achieved in a bipolar PAL circuit. This family of PALs is 100% functionally and pin-for-pin compatible with the industry standard 'PAL16L8, 'PAL16R4, 'PAL16R6, and 'PAL16R8. The Texas Instruments IMPACT-X™ (Enhanced Implanted Advanced Composed Technology) fabrication process has been employed to ensure this ultra-high-performance operation. This process combines the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

All of the register outputs are set to a low level during power-up. Extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

The TIBPAL16' C series is characterized for operation from 0°C to 75°C. The TIBPAL16' M series is characterized for operation over the full military temperature range of −55°C to 125°C.

These devices are covered by U.S. Patent Number 4,410,987.
IMPACT-X™ is a trademark of Texas Instruments Incorporated.
PAL® is a registered trademark of Monolithic Memories, Inc.
†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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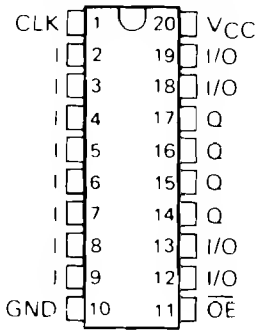
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TIBPAL16R4'
C SUFFIX . . . J OR N PACKAGE
M SUFFIX . . . J PACKAGE
(TOP VIEW)



TIBPAL16R4'
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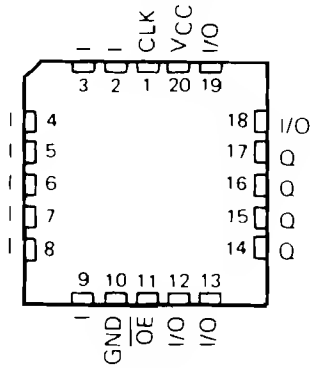
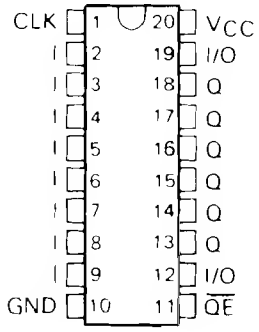
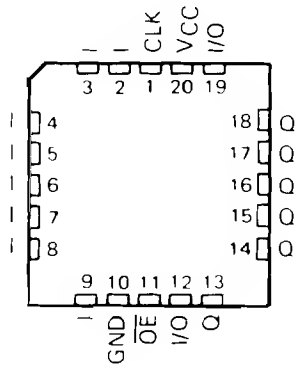
M SUFFIX . . . FK PACKAGE
(TOP VIEW)



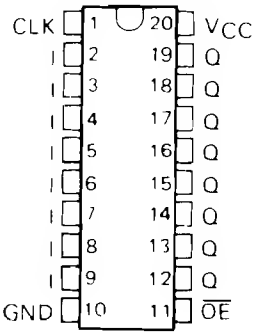
TIBPAL16R6'
C SUFFIX . . . J OR N PACKAGE
M SUFFIX . . . J PACKAGE
(TOP VIEW)



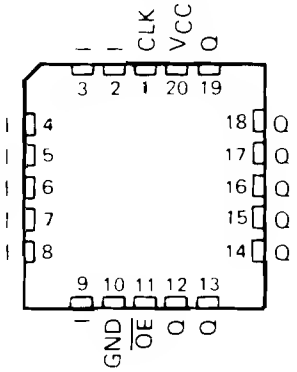
TIBPAL16R6'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE
(TOP VIEW)



TIBPAL16R8'
C SUFFIX . . . J OR N PACKAGE
M SUFFIX . . . J PACKAGE
(TOP VIEW)



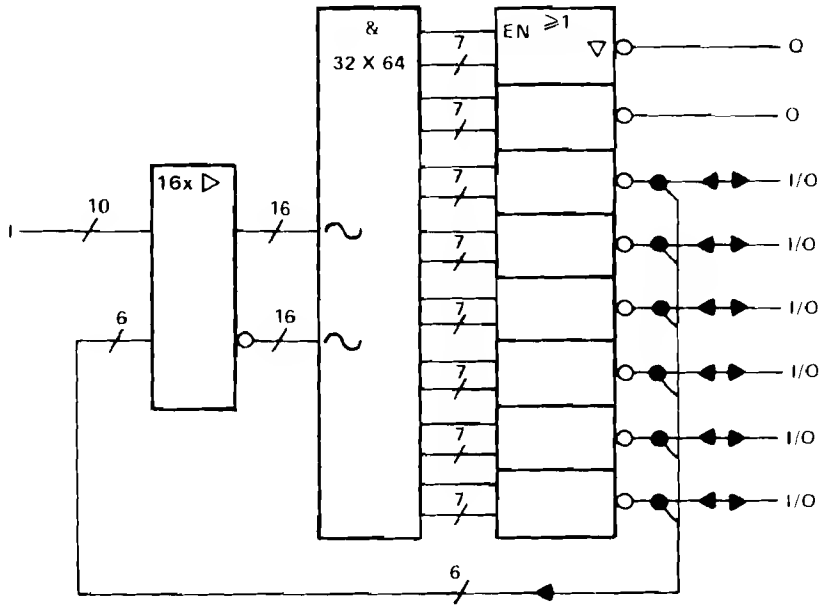
TIBPAL16R8'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE
(TOP VIEW)



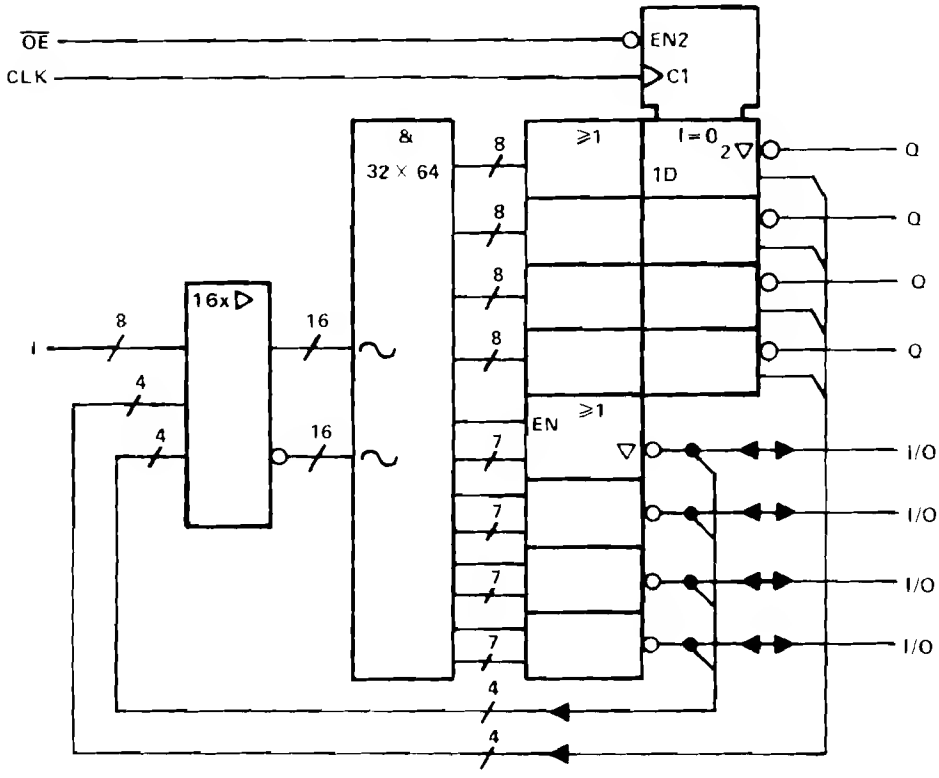
Pin assignments in operating mode

functional block diagrams (positive logic)

'PAL16L8



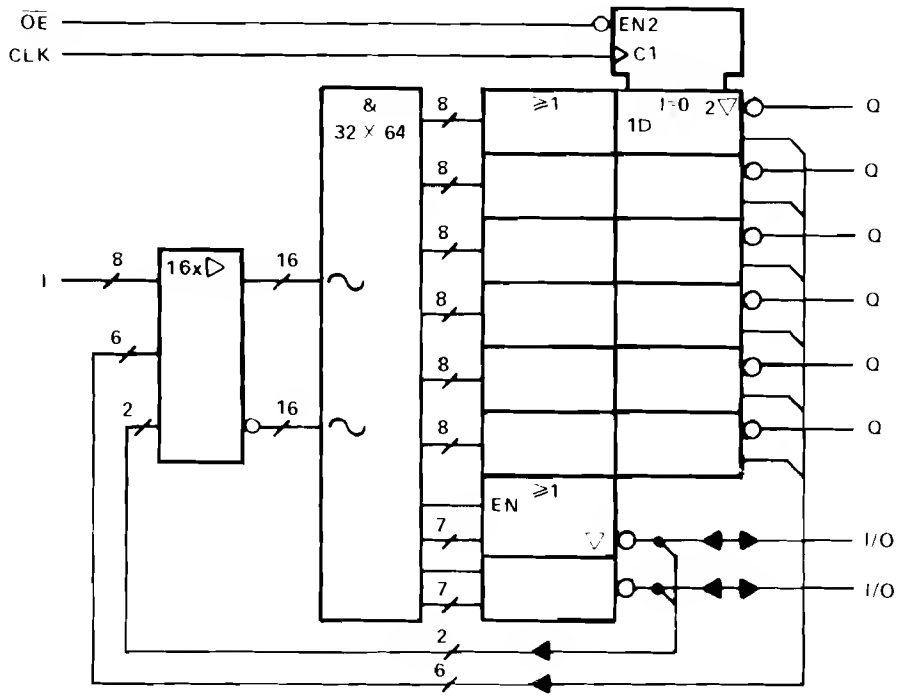
'PAL16R4



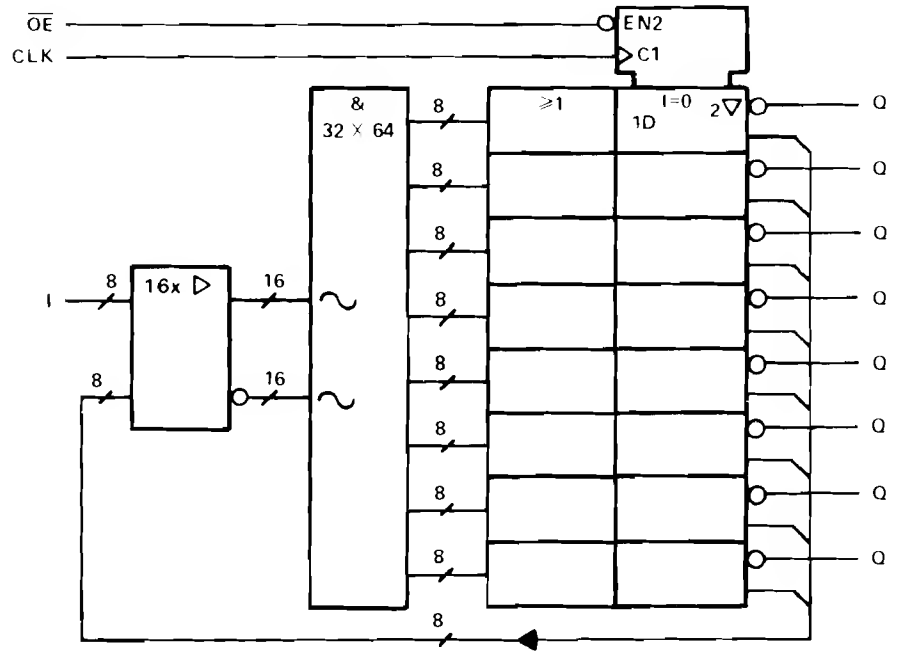
~ denotes fused inputs

functional block diagrams (positive logic)

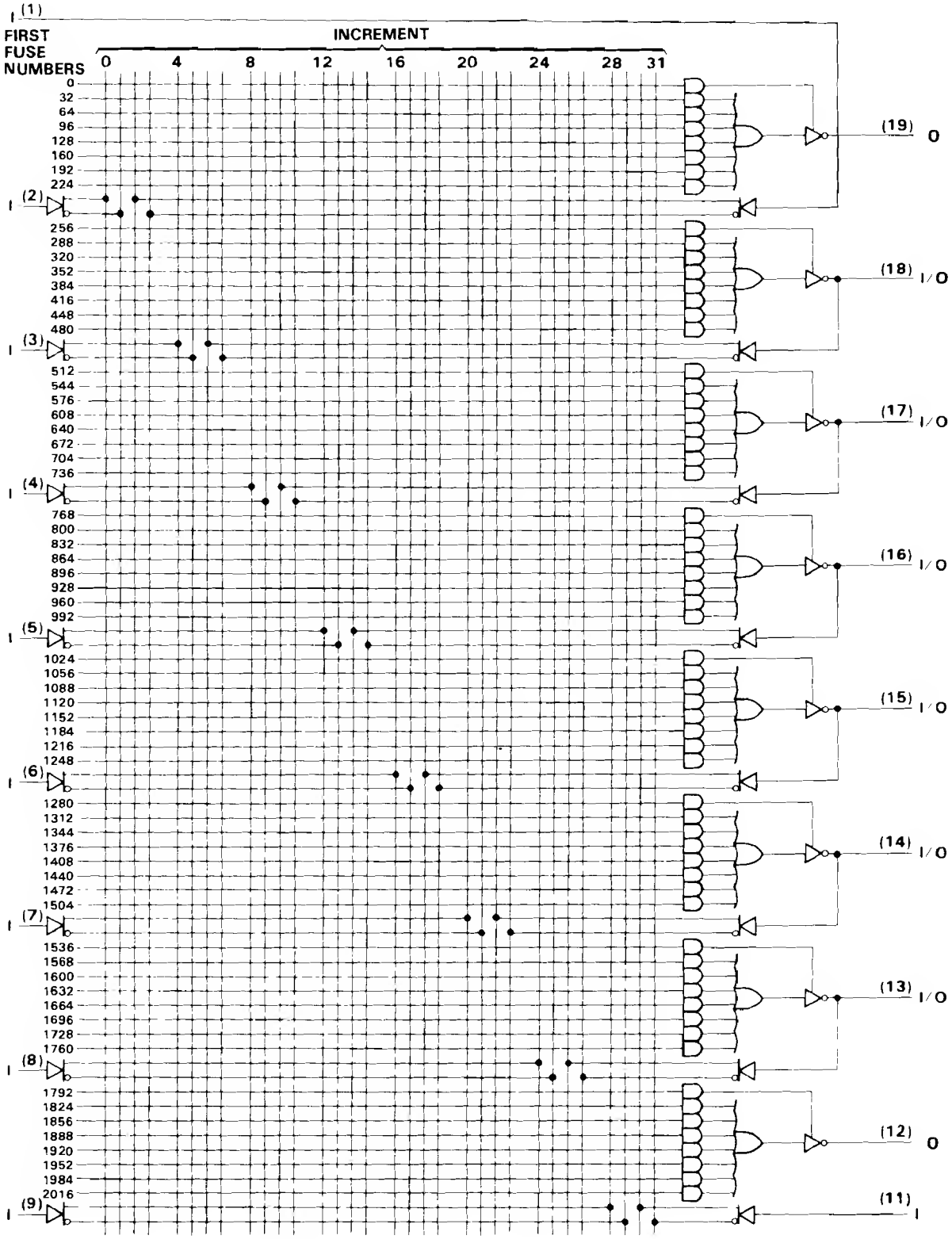
'PAL16R6



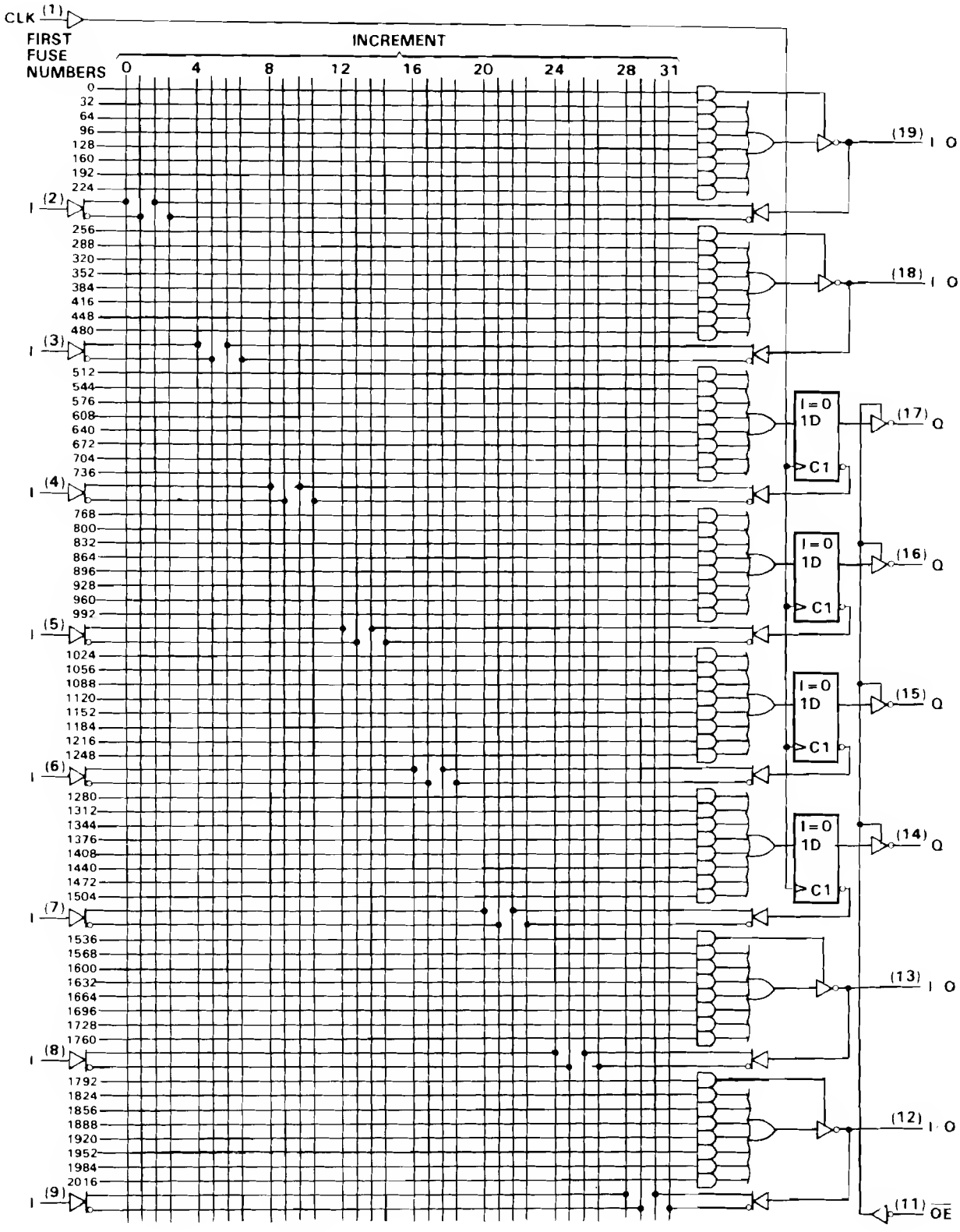
'PAL16R8



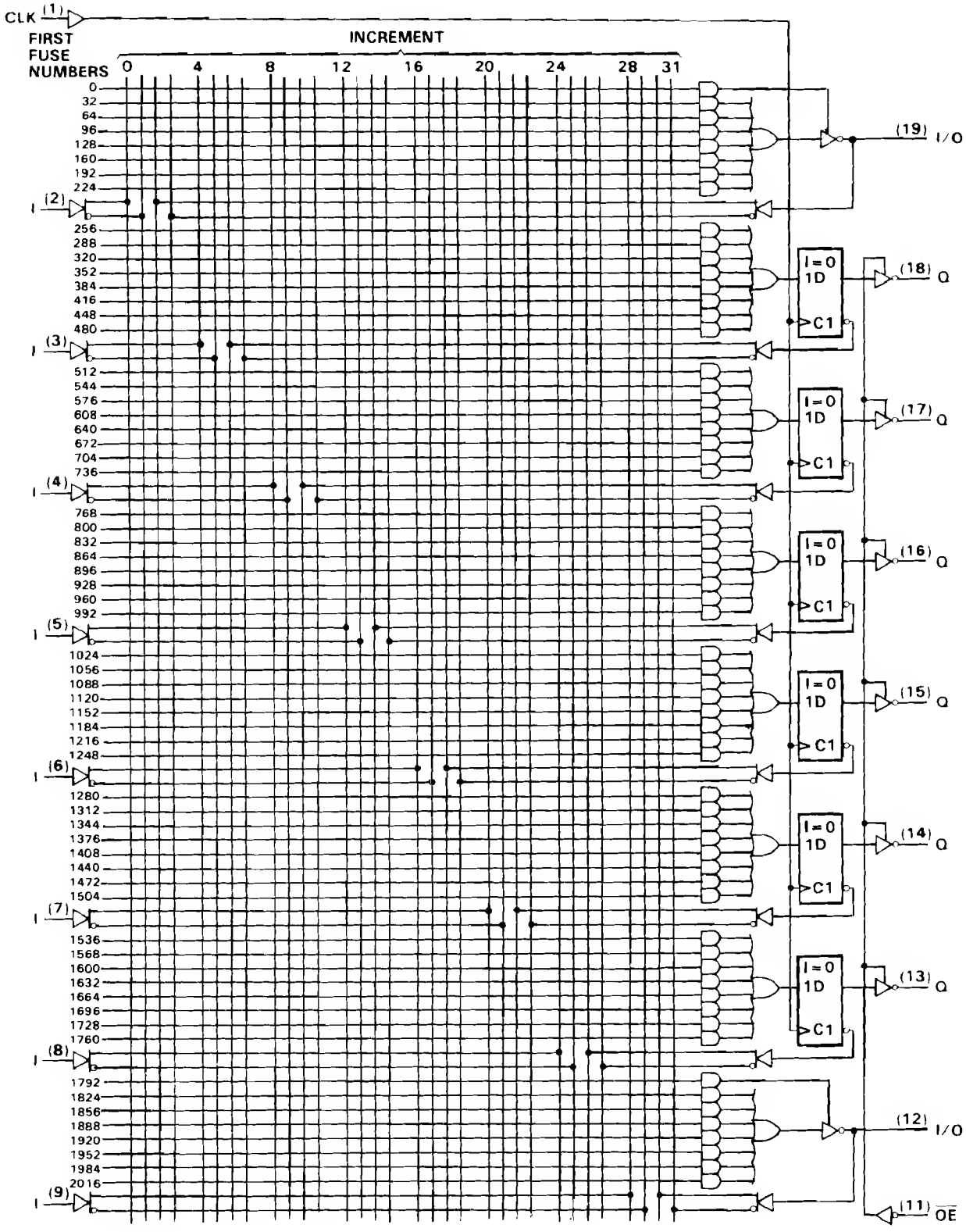
~ denotes fused inputs



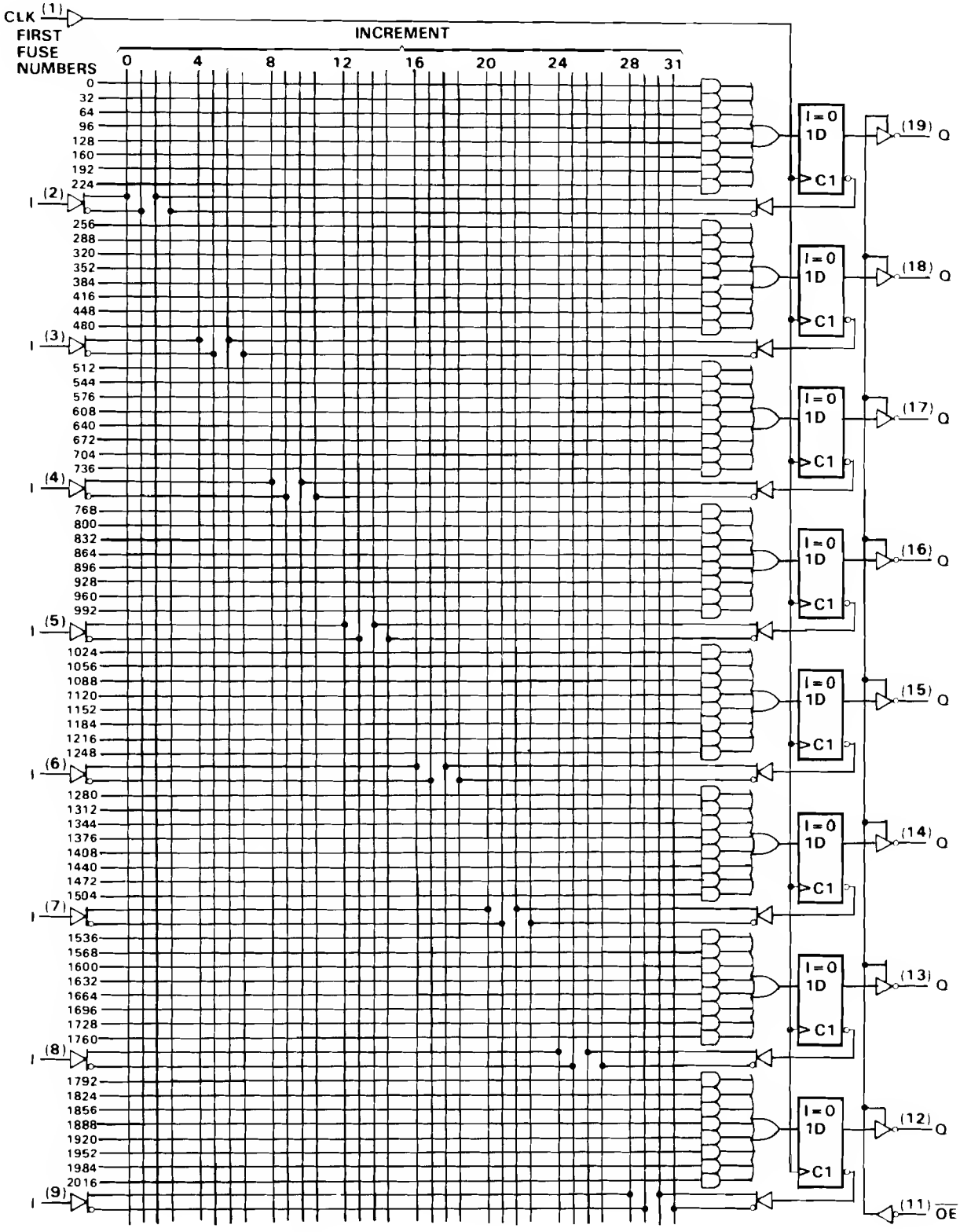
Fuse number = First Fuse number + Increment



Fuse number = First Fuse number − Increment



Fuse number = First Fuse number + Increment



Fuse number = First Fuse number + Increment

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

	PARAMETER	MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2		5.5	V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−3.2	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature	0	25	75	°C

electrical characteristics over recommended free-air operating temperature range

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_I = −18 mA			−0.8	−1.5	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = −3.2 mA		2.4			V
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 24 mA			0.3	0.5	V
I_{OZH}	V_{CC} = 5.25 V,	V_O = 2.7 V				100	μA
I_{OZL}	V_{CC} = 5.25 V,	V_O = 0.4 V				−100	μA
I_I	V_{CC} = 5.25 V,	V_I = 5.5 V				0.1	mA
I_{IH}‡	V_{CC} = 5.25 V,	V_I = 2.7 V				25	μA
I_{IL}‡	V_{CC} = 5.25 V,	V_I = 0.4 V				−0.25	mA
I_{OS}§	V_{CC} = 5.25 V,	V_O = 0.5 V		−30	−70	−130	mA
I_{CC}	V_{CC} = 5.25 V,	V_I = 0,	Outputs open			180	mA
C_i	f = 1 MHz,	V_I = 2 V			5		pF
C_o	f = 1 MHz,	V_O = 2 V			6		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed 1 second. Set V_O at 0.5 V to avoid test equipment ground degradation

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd}	I, I/O	O, I/O	FN package	R1 = 200 Ω, R2 = 200 Ω, See Figure 4		5	ns
			JT and NT packages with up to 4 outputs switching			5	ns
			JT and NT packages with more than 4 outputs switching			5.5	ns
t_{en}	I, I/O	O, I/O				7	ns
t_{dis}	I, I/O	O, I/O				7	ns

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−3.2	mA
I_{OL}	Low-level output current				24	mA
f_{clock}	Clock frequency		0		125	MHz
t_w	Pulse duration, clock	High	4			ns
		Low	4			ns
t_{su}	Setup time, input or feedback before CLK↑		4			ns
t_h	Hold time, input or feedback after CLK↑		0			ns
T_A	Operating free-air temperature		0	25	75	°C

PRODUCT PREVIEW

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V, I_I = −18 mA			−0.8	−1.5	V
V_{OH}		V_{CC} = 4.75 V, I_{OH} = −3.2 mA		2.4			V
V_{OL}		V_{CC} = 4.75 V, I_{OL} = 24 mA			0.3	0.5	V
I_{OZH}	Q outputs	V_{CC} = 5.25 V, V_O = 2.7 V				20	μA
	I/O ports					100	
I_{OZL}	Q outputs	V_{CC} = 5.25 V, V_O = 0.4 V				−20	μA
	I/O ports					−100	
I_I		V_{CC} = 5.25 V, V_I = 5.5 V				0.1	mA
I_{IH}‡		V_{CC} = 5.25 V, V_I = 2.7 V				25	μA
I_{IL}‡		V_{CC} = 5.25 V, V_I = 0.4 V				−0.25	mA
I_{OS}§		V_{CC} = 5.25 V, V_O = 0.5 V		−30	−70	−130	mA
I_{CC}		V_{CC} = 5.25 V, V_I = 0,	Outputs open			180	mA
C_i		f = 1 MHz, V_I = 2 V			5		pF
C_o		f = 1 MHz, V_O = 2 V			6		pF
C_{clk}		f = 1 MHz, V_{CLK} = 2 V			6		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed 1 second. Set V_O at 0.5 V to avoid test equipment ground degradation

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO		TEST CONDITIONS	MIN	MAX	UNIT
f_{max}¶	without feedback			R1 = 200 Ω, R2 = 200 Ω, See Figure 4	125		MHz
	with internal feedback (counter configuration)				125		
	with external feedback				115		
t_{pd}	I, I/O	O, I/O	FN package			5	ns
			JT and NT packages with up to 4 outputs switching			5	ns
			JT and NT packages with more than 4 outputs switching			5.5	ns
t_{pd}	CLK↑	Q				4	ns
t_{pd}	CLK	Internal feedback				3	ns
t_{en}	OE↓	Q				6	ns
t_{dis}	OE↑	Q				6	ns
t_{en}	I, I/O	I/O				7	ns
t_{dis}	I, I/O	I/O				7	ns
t_{skew}	Skew between registered outputs						ns

¶ See "f_{max} Specifications" near the end of this data sheet.

PRODUCT PREVIEW

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−3.2	mA
I_{OL}	Low-level output current				24	mA
f_{clock}	Clock frequency		0		125	MHz
t_w	Pulse duration, clock	High	4			ns
		Low	4			ns
t_{su}	Setup time, input or feedback before CLK↑		4			ns
t_h	Hold time, input or feedback after CLK↑		0			ns
T_A	Operating free-air temperature		0	25	75	°C

PRODUCT PREVIEW

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

electrical characteristics over recommended free-air operating temperature range

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_I = −18 mA		−0.8	−1.5	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = −3.2 mA	2.4			V
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 24 mA		0.3	0.5	V
I_{OZH}	V_{CC} = 5.25 V,	V_O = 2.7 V			20	μA
I_{OZL}	V_{CC} = 5.25 V,	V_O = 0.4 V			−20	μA
I_I	V_{CC} = 5.25 V,	V_I = 5.5 V			0.1	mA
I_{IH}	V_{CC} = 5.25 V,	V_I = 2.7 V			25	μA
I_{IL}	V_{CC} = 5.25 V,	V_I = 0.4 V			−0.25	mA
I_{OS}‡	V_{CC} = 5.25 V,	V_O = 0.5 V	−30	−70	−130	mA
I_{CC}	V_{CC} = 5.25 V, Outputs open,	V_I = 0, $\overline{OE}$ at V_{IH}			180	mA
C_i	f = 1 MHz,	V_I = 2 V		5		pF
C_o	f = 1 MHz,	V_O = 2 V		6		pF
C_{clk}	f = 1 MHz,	V_{CLK} = 2 V		6		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed 1 second. Set V_O at 0.5 V to avoid test equipment ground degradation

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	MAX	UNIT
f_{max}§	without feedback		R1 = 200 Ω, R2 = 200 Ω, See Figure 4	125		MHz
	with feedback (counter configuration)			125		
	with external feedback			115		
t_{pd}	CLK↑	Q			4	ns
t_{pd}	CLK	Internal feedback			3	ns
t_{en}	OE↓	Q			6	ns
t_{dis}	OE↑	Q			6	ns
t_{skew}	Skew between registered outputs					ns

§See "f_{max} Specifications" near the end of this data sheet.

PRODUCT PREVIEW

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage (see Note 2)		2		5.5	V
V_{IL}	Low-level input voltage (see Note 2)				0.8	V
I_{OH}	High-level output current				−2	mA
I_{OL}	Low-level output current				12	mA
f_{clock}	Clock frequency		0		100	MHz
t_w	Pulse duration, clock (see Note 2)	High	6			ns
		Low	6			ns
t_{su}	Setup time, input or feedback before CLK↑		7			ns
t_h	Hold time, input or feedback after CLK↑		0			ns
T_A	Operating free-air temperature		−55	25	125	°C

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−0.8	−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −2 mA		2.4	3.2		V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA			0.3	0.5	V
I_{OZH}	O, Q outputs	V_{CC} = 5.5 V,	V_O = 2.7 V				20	μA
	I/O ports						100	
I_{OZL}‡	O, Q outputs	V_{CC} = 5.5 V,	V_O = 0.4 V				−20	μA
	I/O ports						−250	
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V				1	mA
I_{IH}	I/O ports	V_{CC} = 5.5 V,	V_I = 2.7 V				100	μA
	All others						25	
I_{IL}‡		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.08	−0.25	mA
I_{OS}§		V_{CC} = 5 V,	V_O = 0.5 V		−30	−70	−130	mA
I_{CC}		V_{CC} = 5.5 V,	Outputs open,	T_A = 25°C and 125°C		120	180	mA
		V_I = 0 V,	$\overline{OE}$ = V_{IH}	T_A = −55°C				
C_i		f = 1 MHz,	V_I = 2 V			5		pF
C_o		f = 1 MHz,	V_O = 2 V			6		pF
C_{clk}		f = 1 MHz,	V_{CLK} = 2 V			6		pF

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡I/O leakage is the worst case of I_{OZL} and I_{IL} or I_{OZH} and I_{IH}, respectively.
§Not more than one output should be shorted at a time, and duration of the short circuit should not exceed 1 second. Set V_O at 0.5 V to avoid test equipment ground degradation.

PRODUCT PREVIEW

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

switching characteristics over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	MAX	UNIT
f_{max}§	without feedback		R1 = 390 Ω, R2 = 750 Ω, See Figure 4	100		MHz
	with internal feedback (counter configuration)			100		
	with external feedback			74		
t_{pd}	I, I/O	O, I/O				ns
t_{pd}	CLK	Q				ns
t_{en}	OE↓	Q				ns
t_{dis}	OE↑	Q				ns
t_{en}	I, I/O	O, I/O				ns
t_{dis}	I, I/O	O, I/O				ns

§See "f_{max} Specifications" near the end of this data sheet. f_{max} does not apply for TIBPAL20L8'.

PRODUCT PREVIEW

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

programming information

Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

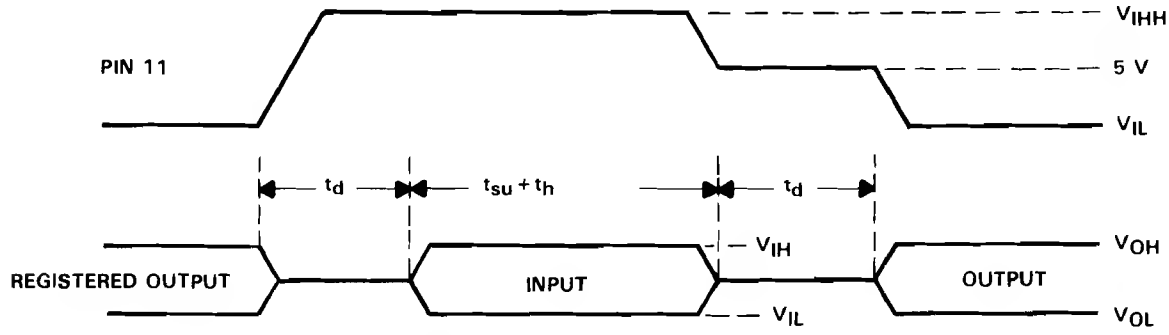
Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

asynchronous preload procedure for registered outputs (see Note 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

Step 1. With V_{CC} at 5 volts and Pin 1 at V_{IL}, raise Pin 11 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Lower Pin 11 to 5 V.
Step 4. Remove output voltage, then lower Pin 11 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

asynchronous preload waveforms (see Note 3)



NOTE 3: $t_d = t_{su} = t_h$ = 100 ns to 1000 ns
V_{IHH} = 10.25 V to 10.75 V

f_{max} SPECIFICATIONS

f_{max} without feedback, see Figure 1

In this mode, data is presented at the input to the flip-flop and clocked through to the Q output with no feedback. Under this condition, the clock period is limited by the sum of the data setup time and the data hold time ($t_{su} + t_h$). However, the minimum f_{max} is determined by the minimum clock period ($t_w$high + $t_w$low).

Thus, f_{max} without feedback $= \dfrac{1}{(t_w \text{ high} + t_w \text{ low})}$ or $\dfrac{1}{(t_{su} + t_h)}$

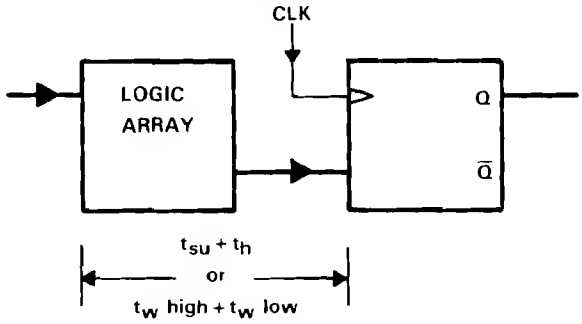


FIGURE 1. f_{max} WITHOUT FEEDBACK

f_{max} with internal feedback, see Figure 2

This configuration is most popular in counters and on-chip state-machine designs. The flip-flop inputs are defined by the device inputs and flip-flop outputs. Under this condition, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic array to the inputs of the next flip-flop.

Thus, f_{max} with internal feedback $= \dfrac{1}{(t_{su} + t_{pd} \text{ CLK-to-FB})}$

Where t_{pd} CLK-to-FB is the deduced value of the delay from CLK to the input of the logic array.

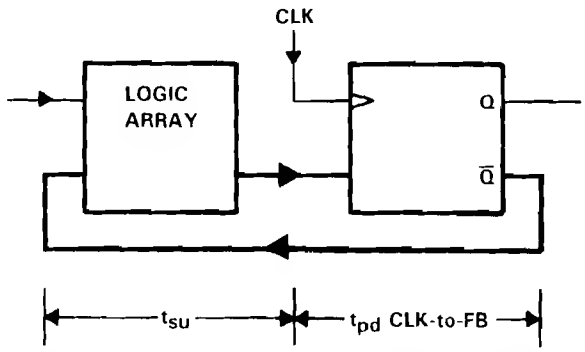


FIGURE 2. f_{max} WITH INTERNAL FEEDBACK

f_{max} SPECIFICATIONS

f_{max} with external feedback, see Figure 3

This configuration is a typical state-machine design with feedback signals sent off-chip. This external feedback could go back to the device inputs or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input and setup time for the external signals ($t_{su} + t_{pd}$ CLK-to-Q).

Thus, f_{max} with external feedback $= \dfrac{1}{(t_{su} + t_{pd} \text{ CLK-to-Q})}$.

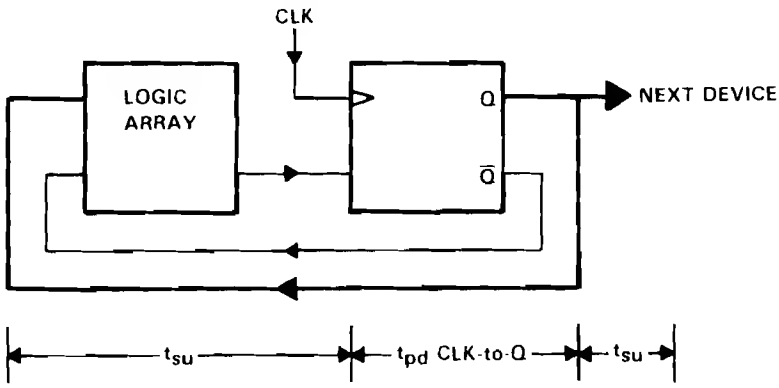
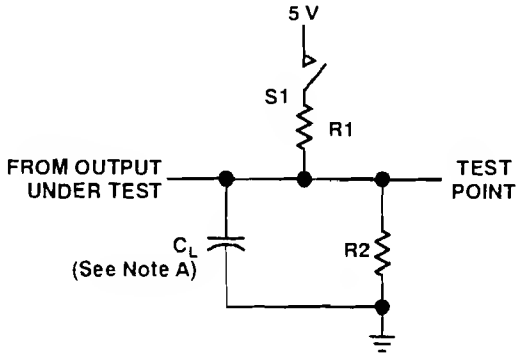
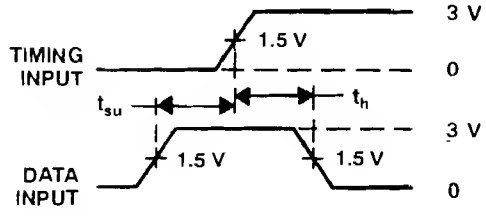


FIGURE 3. f_{max} WITH EXTERNAL FEEDBACK

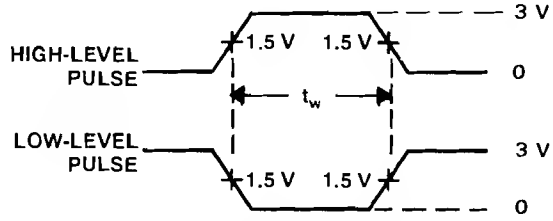
PARAMETER MEASUREMENT INFORMATION



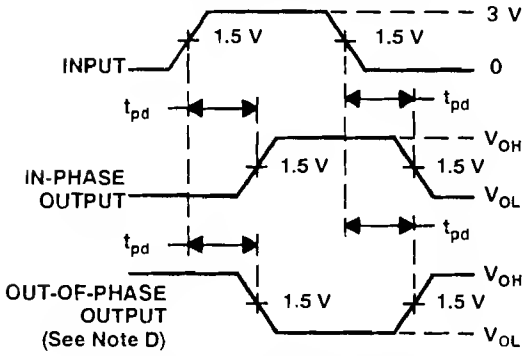
LOAD CIRCUIT FOR 3-STATE OUTPUTS



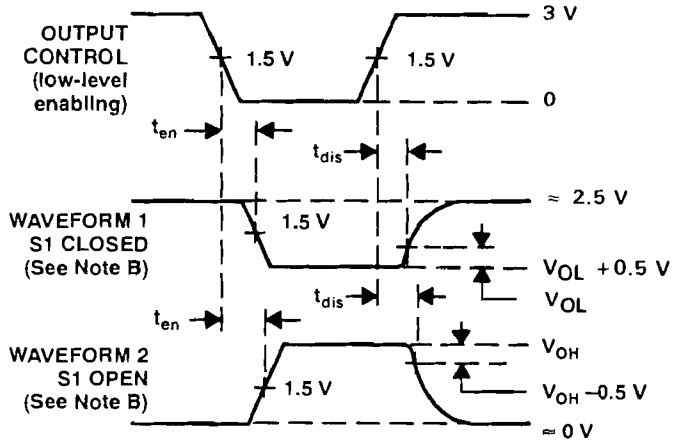
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: For C suffix, PRR ≤ 1 MHz, $t_r = t_f \leq 2$ ns, duty cycle = 50%; For M suffix, PRR ≤ 10 MHz, $t_r = t_f \leq 2$ ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

FIGURE 4. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

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